

What is claimed is:

1. An apparatus, for use in a semiconductor memory device, for controlling a core voltage generator for providing
5 a core voltage to be coupled to a bit line sensing amplifier, comprising:

a bit line sensing start signal controller for receiving a bit line sensing start signal to generate a delayed bit line sensing start control signal in response to a refresh signal;

10 a core overdriving controller for generating an overdriving control signal in response to the delayed bit line sensing start signal; and

15 a core voltage generator for generating the core voltage in response to the delayed bit line sensing start signal and the overdriving control signal to thereby provide core voltage to the bit line sensing amplifier after a predetermined delayed time from the bit line sensing start control signal.

2. The apparatus as recited in claim 1, wherein the bit
20 line sensing start signal controller includes:

a first path for passing the bit line sensing start signal;

25 a second path having a delay block for delaying the bit line sensing start signal for the predetermined delayed time to output the delayed bit line sensing start signal; and

a selection block, in response to the refresh signal, for selectively outputting the delayed bit line sensing signal

as an output signal.

3. The apparatus as recited in claim 2, wherein the selection block includes:

5 a first transferring gate connected to the first path to be turned off in response to the refresh signal; and
a second transferring gate connected to the second path to be turned on in response to the refresh signal.

10 4. The apparatus as recited in claim 3, wherein each of the first and the second transferring gates includes an NMOS transistor and a PMOS transistor.

15 5. The apparatus as recited in claim 2, wherein the second path includes an inverter chain for delaying the bit line sensing start signal for the predetermined delay time.

20 6. The apparatus as recited in claim 3, wherein the over driving controller includes a NAND gate and an inverter chain, wherein the output signal is coupled to one input of the NAND gate and the inverter chain, and the delayed output from the inverter is coupled to the other input of the NAND gate.

25 7. The apparatus as recited in claim 3, wherein the over driving controller includes a capacitor structure.

8. A method for generating a core voltage to be coupled

to a bit line sensing amplifier for use in a semiconductor memory device, comprising a step of:

delaying a bit line sensing start signal to generate the delayed bit line sensing start signal in response to a refresh signal;

generating an overdriving control signal in response to the delayed bit line sensing start signal; and

generating a core voltage in response to the delayed bit line sensing start signal and the over driving control signal to thereby provide the core voltage to the bit line sensing amplifier after a predetermined delayed time from the bit line sensing start control signal.

9. A semiconductor memory device, having a circuit for controlling a core voltage generator for providing a core voltage to be coupled to a bit line sensing amplifier, comprising:

a bit line sensing start signal controller for receiving a bit line sensing start signal to generate a delayed bit line sensing start control signal in response to a refresh signal;

a core overdriving controller for generating an overdriving control signal in response to the delayed bit line sensing start signal; and

a core voltage generator for generating the core voltage in response to the delayed bit line sensing start signal and the overdriving control signal to thereby provide core voltage to the bit line sensing amplifier after a predetermined

delayed time from the bit line sensing start control signal.

10. The semiconductor memory device as recited in claim
9, wherein the bit line sensing start signal controller
5 includes:

a first path for passing the bit line sensing start
signal;

a second path having a delay block for delaying the bit
line sensing start signal for the predetermined delayed time
10 to output the delayed bit line sensing start signal; and

a selection block, in response to the refresh signal,
for selectively outputting the delayed bit line sensing signal
as an output signal.

15 11. The semiconductor memory device as recited in claim
10, wherein the selection block includes:

a first transferring gate connected to the first path to
be turned off in response to the refresh signal; and

a second transferring gate connected to the second path
20 to be turned on in response to the refresh signal.

12. The semiconductor memory device as recited in claim
11, wherein each of the first and the second transferring
gates includes an NMOS transistor and a PMOS transistor.

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13. The semiconductor memory device as recited in claim
10, wherein the second path includes an inverter chain for

delaying the bit line sensing start signal for the predetermined delay time.

14. The semiconductor memory device as recited in claim 5 11, wherein the over driving controller includes a NAND gate and an inverter chain, wherein the output signal is coupled to one input of the NAND gate and the inverter chain, and the delayed output from the inverter is coupled to the other input of the NAND gate.

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15. The apparatus as recited in claim 11, wherein the over driving controller includes a capacitor structure.